

**METHOD AND APPARATUS FOR OPTIMIZING THE
TIMING OF INTEGRATED CIRCUITS**

ABSTRACT OF THE DISCLOSURE

Integrated circuits are designed having
5 optimal signal timing between and among cells. A set
of identities are generated corresponding to logic
operations and to library cells in technology basis.
A resynthesis window is created for the identities
having less than a predetermined depth of critical
10 variables. Logic equations of the resynthesis window
are transformed using the identities, and the
resynthesized window area is optimized.

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